

## **REMARKS**

This application has not been examined. The following amendment is respectfully submitted to place the application in better form prior to examination. The specification has been corrected for minor errors. Claims 6-9, 17 and 23 have been amended. Claims 1-32 remain active in the application. No new matter has been added to the application.

### **Specification**

A number of paragraphs have been amended to replace uses of the word “effective” with “valid.” It is clear from the description of the cache that what was meant was whether a cache element contained valid data or not. This concept was not, however, translated precisely in the original translation to English. The corrections to the specification substitute the common English word for this concept, and add no new matter to the application.

### **Drawings**

Figure 3 has been amended to show the connection for reading data out of CMB2 and into an SMB. This connection is fully described in the specification see, (e.g. pp13/ll.17-22), but was inadvertently omitted from the originally submitted Figure 3. A proposed drawing correction accompanies this response.

### **Claims**

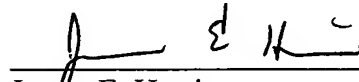
Claims 6, 17, and 23 have been amended for clarity by changing "effective" to "valid". Valid is the more appropriate term that is more commonly used by those skilled in the art the invention.

Claims 6-9 have been amended to more clearly state describe the tag memory control unit. The specification clearly describes a tag memory control unit that stores both validity and address information for a location corresponding to each possible sub memory block lower address (see, e.g. pp.7/ll.20-pp.8/ll.3). This change is fully supported by the specification and no new matter has been added to the application.

Accordingly, applicants request that the amendment be entered and the application be allowed.

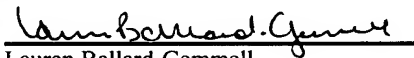
Respectfully submitted,

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Lauren Ballard-Gemmell

## **APPENDIX**

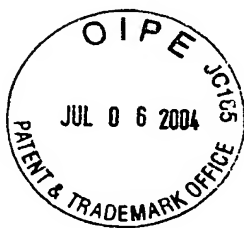


FIG. 3

